In the United States Patent and Trademark Office

Appellant:	David R. Baldwin
Application No.:	09/591,225
Filing Date:	June 9, 2000
Examiner:	Richer, Aaron M.
Title:	Graphic Memory Management with Invisible Hardware-Managed Page Faulting
Art Unit:	2671
Docket No.:	TD-155

For: **Graphics Memory Management with Invisible Hardware-Managed Page Faulting**

REPLY BRIEF

Honorable Commissioner of Patents and Trademarks
Alexandria, VA 22313

Sir:

Enclosed is a Reply Brief on the above captioned case. This is in reply to Examiner Richer's Answer of September 26, 2007.

Any extension of time necessary for consideration of this appeal is also hereby requested. However, the Commissioner is authorized to charge any fees, or credit any overpayment, to Deposit Account Number 07-2320.

Reply Brief begins on page 2 of this document.

RESPONSE TO NEW ARGUMENT

On Page 4 Paragraph 1 in Section (10) A1 of the Examiner's Answer of September 26, 2007, Examiner Richer makes a new argument asserting that there are "many similarities" between the "TLB miss" of Kaiser *et al.* and the "page fault" of the present Application. The Examiner also ends that paragraph by stating that in Kaiser *et al.*, "The host processor is only involved if no entry is found in the system page table."

First, the Applicant does not agree that it is proper compare the similarities of a "TLB miss" and a "page fault" using Kaiser *et al.* That reference teaches how to handle a TLB miss at Col. 5 Line 46 through Col 6 Line 2. That reference also clearly states at Col. 6 Lines 3-4: "Since memory controller **204** is not a processor, it cannot deal directly with a page fault." Clearly Kaiser *et al.* had no need to compare or equate a TLB miss and a page fault. Clearly Kaiser calls a TLB miss a "TLB miss" and a page fault a "page fault." Clearly Kaiser *et al.* teaches they are different events and blatantly admits that they cannot manage page faults directly without involving the host processor. Applicant also questions whether Examiner Richer may have been commingling issues of virtual memory management with those of cache management.

Second, the Appellant also roundly disagrees with the assertion that the host processor of Kaiser *et al*. is only involved if no entry is found in the page table. For example, in Kaiser *et al.* at Col. 6 Lines 14-29, they describe the situation wherein their graphics engine **206** updates a page in page table buffer **226** but that same page had already been invalidated by processor **12**. In such an instance, an entry for a page is in-fact found in buffer **226** by the address translation logic, but it is forced to trigger a page fault to processor **12,** based on the "C" bit for that entry in the page table not being set. This causes processor **12** to rerun the faulting

address. Thus, this is a situation where the host processor is involved even when an entry is found in the page table.

In contrast, the present innovations in-fact ***do deal directly with a page fault***. Examiner Richer is directed to Page 8 Lines 12-14 of the present Application:

> "When a logical page fault occurs and the page of texture is in the second level of memory (i.e. the host's physical memory) it will be fetched in automatically by the graphics memory manager, and the host is not aware anything has happened."

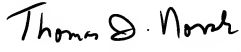
REQUESTED RELIEF

For the reasons advanced above, Appellant respectfully contends that all claims are patentable. Therefore, reversal of the rejections is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection of this paper, including extension of time fees, to Deposit Account 07-2320 and please credit any excess fees to such deposit account.

October 26, 2007

Respectfully submitted,



Thomas J. Novak, Reg. No. 57,683
Patent Agent for the Appellant

Customer Number 29106
Groover & Associates
PO Box 802889
Dallas, TX 75380
Tel: 972-980-5840
fax: 972-980 -5841